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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,087	03/31/2004	Takahiro Ochiai	HITA.0535	5095
7590		05/11/2007		
Stanley P. Fisher Reed Smith LLP Suite 1400 3110 Fairview Park Drive Falls Church, VA 22042-4503				
			EXAMINER SANEI, HANA ASMAT	
			ART UNIT 2879	PAPER NUMBER
			MAIL DATE 05/11/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/813,087

Applicant(s)

OCHIAI ET AL.

Examiner

Hana A. Sanei

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 26 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 2-6, 9 and 10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-4 and 10 is/are allowed.
- 6) ☒ Claim(s) 5-6, 9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 February 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on 3/26/07 has been entered.

Cancellation of claims 1, 7-8 has been entered.

Claims 2-6, 9-10 are pending in the instant application.

### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 5 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Dojo et al (US 2002/0132385 A1).

Regarding Claim 5, Dojo teaches signal lines (131, signal line connection layer, see at least Fig. 13) which are formed on an upper surface side of the substrate (101) to

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provide a display region; semiconductor layers (123) which are formed below the signal lines (131) byway of a first insulation film (127, interlayer dielectric layer) such that the semiconductor layers traverse the signal lines at terminal portions of the signal lines in a periphery of the substrate; a second insulation film (141, see final product of device, Fig. 6) which is formed on top of the substrate to cover the signal lines and in which holes (153, 154, 155, & 156) are formed above regions thereof where the semiconductor layers are formed; and conductive layers (125a & 125b) which have respective sides thereof in the extension direction of the signal lines arranged at both sides of the signal lines and are connected with respective semiconductor layers, wherein the semiconductor layers are exposed at positions of the holes (that the semiconductor layer 123 ceases at the beginning of the thru-hole 154, it is thereby "exposed" to the positions of that respective hole), wherein the display region includes thin film transistors (TFT Region, Fig. 13), and a material of the semiconductor layers in the periphery of the substrate (low resistance semiconductor material, [0054]) is equal to a material of the semiconductor layers of the thin film transistors (low resistance semiconductor material, [0097]) in the display region.

Regarding Claim 9, Dojo teaches gate signal lines (included in 111, see at least Fig. 13), drain signal lines (included in 111) and interlayer insulation films (127) which are formed between the respective signal lines (131) are formed on a display region and a material of the second insulation film (141, [0032]) is identical with a material of the interlayer insulation films (127, [0038]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dojo et al (US 2002/0132385 A1) in view of Ono et al (US 6356331 B1) in further view of Ono et al (US 2002/0047970 A1) hereinafter referred to as '970.

Regarding Claims 6, Dojo teaches the invention set forth above (see rejection in Claim 5 above) and further teaches gate signal lines and drain signal lines ([0014], [0041], 111 region, see at least Fig. 13). Dojo lacks the material of the signal lines being equal to a material of the gate signal lines. In the same field of endeavor, Ono teaches the material of the signal lines (CL, Col. 5, lines 22-25) being equal to a material of the gate signal lines (GL) in order to achieve the advantage of preventing an increase in the number of manufacturing steps (Col. 5, lines 25-27). Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the materials, as disclosed by Ono, in the device of Dojo in order to achieve the advantage of preventing an increase in the number of manufacturing steps.

Dojo-Ono lacks the material of the conductive layer being equal to the material of the drain signal lines. In the same field of endeavor, '970 teaches the conductive layer (SD1; [0075]) being equal to the material of the drain signal lines (DL) in order to ensure

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the improvement in reliability of connection with the semiconductor layer AS stated supra ([0075]). Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the materials, as disclosed by Ono, in the device of Dojo in order to ensure the improvement in reliability of connection with the semiconductor layer.

***Allowable Subject Matter***

A. Claim 2-4 are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

The prior art of record teaches a display device comprising: signal lines which are formed on an upper surface side of a substrate to provide a display region; an insulation film which is formed to cover the signal lines except for terminal portions of the signal lines in periphery of the substrate; and conductive layers which extend in an extension direction of the signal lines layers to traverse the terminal portions, wherein a gap is formed in the insulation film and is shaped rectangular, a pair of holes are formed in the signal lines at portions underneath and corresponding to two sides of the gap along the extension direction, and each of the conductive layers is formed on the signal lines and between the pair of holes, while the insulated film is formed on the signal lines and outside of the pair of holes.

However, the prior art of record neither shows nor suggests a motivation for a part of said each conductive layer is formed on the insulating film as set forth in Claim 2.

Claims 3-4 are allowable because of their dependency status from claim 2.

B. Claim 10 is allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

The prior art of record teaches a display device comprising: signal lines which are formed on an upper surface side of a substrate to provide a display region; a first insulation film which is formed between the substrate and the signal lines, a second insulation film which is formed to cover the signal lines except for terminal portions of the signal lines in periphery of the substrate; and conductive layers which extend in the extension direction of the signal lines to traverse the terminal portions, a part of each of the conductive layers is formed on the second insulating film, wherein each of the signal lines branches to three along the extended direction to provide a central portion and two side portions and said each conductive layer is formed on the central portion, and the second insulation film is formed on the side portions.

However, the prior art of record neither shows nor suggests a motivation for a pair of holes are formed among the central portion and the two side portions, and the first insulation film are exposed at positions of the holes as set forth in Claim 10.

#### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hana A. Sanei whose telephone number is (571)-272-8654. The examiner can normally be reached on Monday- Friday, 9 am - 5 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the

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Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

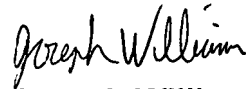
Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).



Hana A. Sanei  
Examiner



**Joseph Williams**  
**Primary Examiner**